1) Half Adder.

2) 1-bit Full Adder.

3) 1-bit Full Adder using Half Adder.

4) 4-bit full adder using Half Adder.

5) Mux using Case statement.

6) Mux using with always block (use logical expression).

7) Mux using Conditional operator.

8) Arithmetic and logic unit.

9) D Flip flop with synchronous reset.

10) D flip flop with asynchronous reset.

11) Sequence Detector using Mealy machine (1101,Non-Overlapping).

12) Sequence Detector using Moore machine (1101,Non-Overlapping).

13) Sequence Detector using Mealy machine (1101, Overlapping).

14) Sequence Detector using Moore machine (1101,Overlapping).

15) Count the no.of 1’s in given input sequence (16-bit input).

16) Binary to gray conversion. It should work for n number of inputs. The number of inputs should be mentioned from test bench.

17) Three-bit up/down counter. It should include a control input called Up/Down. If Up/Down = 0, then the circuit should behave as an up-counter. If Up/Down = 1, then the circuit should behave as a down-counter.

18) Design a 4-bit counter with asynchronous reset, synchronous load and enable inputs. On reset the counter is set to 1000 and counts sequence in the order specified below (top to bottom and loop back). Counter can be loaded with any value present in the sequence. Counter should go back to reset state if loaded with some invalid count. Enable pin can be used to halt the counter if set to 0.

1000

0111

1011

0100

1001

0010

0101

1100

0110

0011

1111

0001

1110

1101

19) Clock divider with input frequency of 400MHz and output of 100MHz.

20) Design a 16-bit parallel in parallel out universal right shift register which performs following operations.

a. Load, Shift enable

b. Logical Left shift

c. Logical Right shift

d. Arithmetic Left shift

e. Arithmetic Right shift

21) N bit universal shift register.

22) 4-bit Linear Feedback Shift Register(LFSR).

23) Write a Verilog/system Verilog description for the following circuit.

24) Single prorated RAM (128x8). Perform Read and write operations.

25) Dual ported RAM (128\*8). Perform Read and write operations.

26) Synchronous FIFO (8x8). Test bench should use task for read and write operations.

27) Asynchronous FIFO (8x8 ) Test bench should use task for read and write operations.

28) Write a Verilog/system Verilog description for the following circuit.

29) Design an 8x8 sequential multiplier. The multiplier has asynchronous reset, synchronous load and output valid signal.

30) 64-bit Pipelined Multiplier (latency should be 6 cycles).